VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please replace the indicated paragraphs as follows:

Paragraph beginning at page 1, line 24 through page 2, line 5:

The delayed clock signal Delayed_clock is fed to a pre-delay/post-delay comparison block 110 that compares the delayed clock signal Delayed_clock with a reference clock signal Reference_clock to thereby determine whether increasing or decreasing the predetermined delay time in required. Through the comparison process, the pre-delay/post-delay/ comparison block 110 generates output signals Add_delay and Subtract_delay that are, in turn, fed back to the controllable delay chain block 100 so as to adjust the delay time.

Paragraph beginning at page 2, line 18:

The pre-delay/post-delay comparison block 210 compares the delayed clock signal Delayed_clock with a reference clock signal Reference_clock so as to determine whether increasing or decreasing the delay time of the delayed clock signal Delayed_clock. is necessary As a result of the comparison process, the pre-delay/post-delay comparison block 210 produces output signals **[Add_delay]** Add_delay_i and **[Sub_delay]** Sub_delay-i to a careful delay controller 220.

Paragraph beginning at page 3, line 12:

As described above, the conventional delay locked loop of Fig. 2 is **[strong]** insensitive to **[a]** noise at the state when the delayed locked loop normally operates and the locking is done. However, there is a disadvantage that it takes a very long time from an initial condition in which the locking is not caused to the locking: That is, since, in order to adjust the time delay, there **[needs]** must be at least two determination processes for the increase or decrease in the delay time generated **[from]** by the pre-delay/post-delay comparison block 210, **[there is a problem making a]** the

time required for the locking may be much longer compared with that of using only one time of determination, as in the delay locked loop of Fig. 1.

Paragraph beginning at page 6, line 2:

The delay locked loop comprises a controllable delay chain block 300 for adjusting a delay time of a clock in response to output signals Add_delay and Subtract_delay of an instant locking delay controller 320, a pre-delay/post-delay comparison block 310 for determining the need for increase **[and]** or decrease of the delay time by comparing a delayed clock signal Delayed_clock **[outputted]** output from the controllable delay chain block 300 with a reference clock signal Reference_clock, and the instant locking delay controller 320 for generating the output signals Add_delay and Subtract_delay by using output signals Add_delay_i and Sub_delay_i of the pre-delay/post-delay comparison block 310, the delayed clock signal Delayed_clock and the reference clock signal Reference__clock, wherein the output signals Add_delay and Subtract_delay are used to control the increase and decrease of the delay time at the controllable delay chain block 300.

Paragraph beginning at page 6, line 18:

[Unlikely to] Unlike the conventional delay locked loop described in Fig. 2, in the inventive delay locked loop shown in Fig. 3, the delayed clock signal Delayed_clock and the reference clock, signal Reference_clock are coupled to both the pre-delay/post-delay comparison block 310 and the instant locking delay controller 320 in parallel. Therefore, the instant locking delay controller 320 can check whether the locking is accomplished or not by comparing the delayed clock signal Delayed_clock and the reference clock signal Reference_clock.

Paragraph beginning at page 13, line 6:

If the careful delay controller 410 is used as soon as the locking detector 430 determines that the locking is accomplished, the entire locking time may become longer. Therefore, information representing that the locking is achieved should be

outputted after a given time. On the other hand, information representing that the locking is not accomplished should be outputted without any delay.

Paragraph beginning at page 13, line 13:

In order to utilize the careful delay controller 410 from the time of outputting a signal depicting that the locking is completed after guaranteeing a much smaller locking error by proceeding a locking procedure without directly using the careful delay controller 410 through a signal representing that the locking is accomplished is generated from the pre-delay/post-delay logic block 550, the output] provide a signal representing an unlocked state without delay while providing a signal representing a locked state only after a given time, output block 800 may be used. Output block 800 receives the time delayed clock signal Delayed-clock and delays the output signal of the pre-delay/post-delay logic block 550 by one or more than one clock cycles. Further, if information showing that the locking is not accomplished at the pre-delay/post-delay logic block 550 is coupled thereto, the output block 800 immediately deactivates the selection signal Rough_lock_flag **[of controlling]** that controls the shift multiplexer to thereby make the careful delay controller 410 not be used.

Paragraph beginning at page 15, line 10:

As described above, in a delay locked loop of a semiconductor memory device in accordance with the present invention, by using **[difference]** different circuits **[in cases]** depending on whether the locking is completed or not, i.e., using the careful delay controller **[When]** when the locking is accomplished and not using the careful delay controller when the locking is not completed, **[there are effects capable of obtaining]** it is possible to obtain a short locking time when the locking is not accomplished and **[reducing]** to reduce an incorrect locking determination due to **[a]** noise **[caused]** by using the careful delay controller when the locking is done.